IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Currently Amended) A method, comprising:

forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate having a gate length less than 0.2 microns without forming a contact hole etch stop liner**; and**

forming the contact hole includes reactive plasma etching through the first insulating layer comprising non-densified doped silicon dioxide.

2. (Cancelled) The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising non-densified doped silicon dioxide.

3. (Previously Amended) The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

4. (Original) The method of claim 3, wherein:

the reactive plasma etching includes introducing CHF_3 and $C_2H_2F_4$ into an etch chamber.

5. (Original) The method of claim 4, wherein:

the flow rate of CHF_3 is less than ten times the flow rate of $C_2H_2F_4$.

6. (Original) The method of claim 5, wherein:

the flow rate of CHF_3 is in the general range of 3-15 standard centimeter cubed per minute (sccm); and

the flow rate of $C_2H_2F_4$ is in the general range of 10-100 sccm.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

7. (Original) The method of claim 3, wherein:

the reactive plasma etching includes exciting a plasma with a radio frequency power source that supplies power in the general range of 100 to 1000 Watts.

8. (Original) The method of claim 3, wherein:

the reactive plasma etching includes an etch time in the general range of 80 to 200 seconds.

9. (Original) The method of claim 3, wherein:

the contact hole is formed on a target object that is biased to an absolute value potential in the general range of 100 to 1500 Volts.

10. (Original) The method of claim 3, wherein:

the reactive plasma etching pressure is in the general range of 20-100 milliTorrs.

11. (Original) The method of claim 3, wherein:

the reactive plasma etching temperature is in the general range of 0-35 °C.

12. (Currently Amended) A method, comprising:

forming a first insulating layer comprising a high density plasma silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight; and

etching a contact hole~~,~~ through ~~a~~ **the** first insulating layer ~~**comprising doped silicon dioxide,**~~ that is self-aligned with respect to a conductive structure that is formed over a substrate and includes insulating sidewalls**, the etching including** ~~**with**~~ an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

13. (Original) The method of claim 12, wherein:

the insulating sidewalls comprise silicon nitride.

14. (Cancelled) The method of claim 12, further including:

forming the first insulating layer comprising a high density plasma silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

15. (Cancelled) The method of claim 12, further including:

forming the conducting structure over a substrate; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

16. (Original) The method of claim 12, further including:

forming a hard etch mask comprising an insulating material over the first insulating layer; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one.

17. (Previously Amended) The method of claim 16, wherein:

the hard etch mask comprises silicon dioxide; and

the first insulating layer comprises phosphorous doped silicon dioxide.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

18. (Currently Amended) A method, comprising:

forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising ~~doped~~ silicon dioxide **having a concentration of phosphorous dopant that is greater than 5% by weight,** the hard mask having openings over a contact hole location; and

forming a contact hole at the contact hole location through the insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures.

19. (Currently Amended) The method of claim 18, wherein:

~~the insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight; and~~

the sidewalls comprise silicon nitride.

20. (Cancelled) The method of claim 18, further including:

forming a hard mask comprising substantially undoped silicate glass over the first insulating layer, the hard mask having openings over a contact hole location.